Electrical Engineering Capstone Project
Non-volatile Resistive Switching Memory Technology

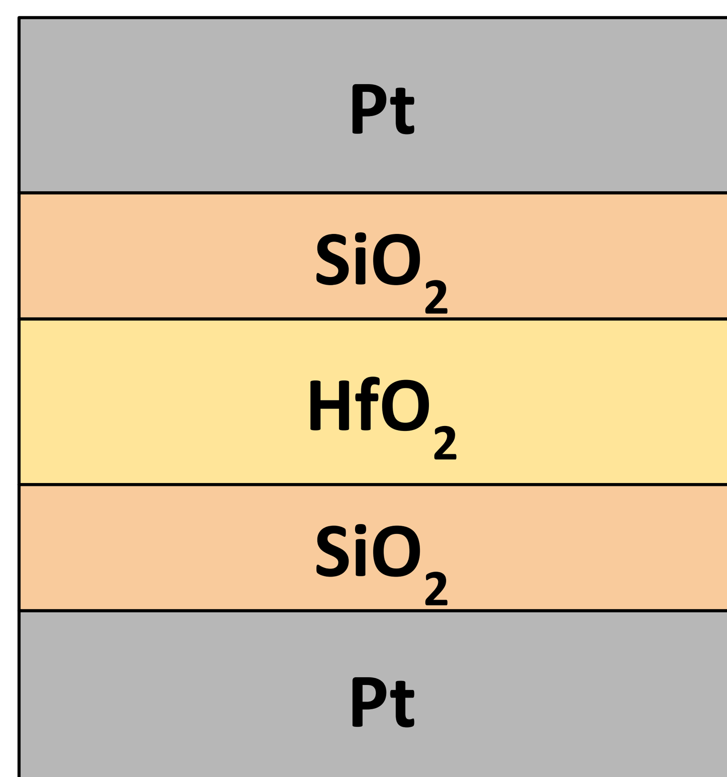
Ethan Morgan, Trevor Smith, Ming-Feng Tsai, Tyler Cloar, Vincent Baer
Mentor: Dr. Ying-Chen Chen

ASU Ira A. Fulton Schools of Engineering
Arizona State University

What is ReRAM?

Resistive Random-Access Memory (RRAM) is a two-terminal, non-volatile memory device that stores data by switching between the High Resistance State (HRS, "0") and the Low Resistance State (LRS, "1").

RRAM is a leading candidate for next-generation memory due to its simple metal-insulator-metal (MIM) structure, fast switching, excellent scalability, and low power consumption — addressing key limitations of conventional charge-based Flash and DRAM.



Resistive Random Access Memory (RRAM)

- Non-Volatile Memory.
- It stores data as resistance.

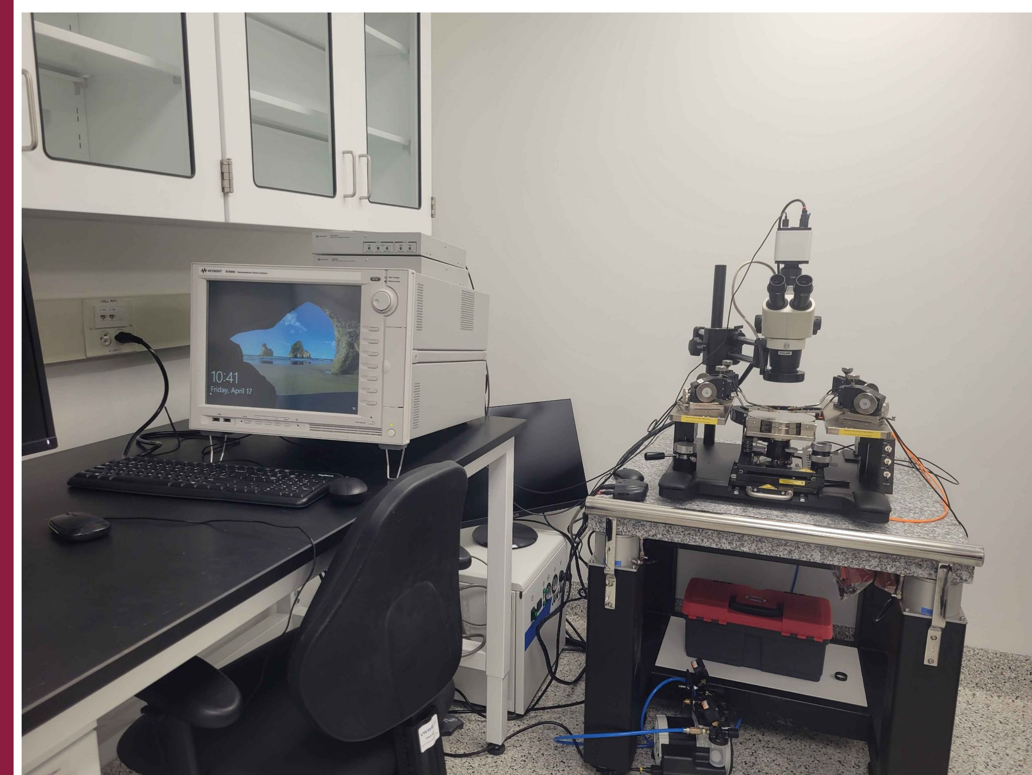
Basic Structure

- Metal/Oxide(Switch Layer)/Metal.
- Filament

Our Device

This project characterizes a novel trilayer RRAM structure: Pt / SiO_2 / HfO_2 / SiO_2 / Pt. The SiO_2 cladding layers serve as a current-limiting interface, potentially enabling self-compliant reset behavior.

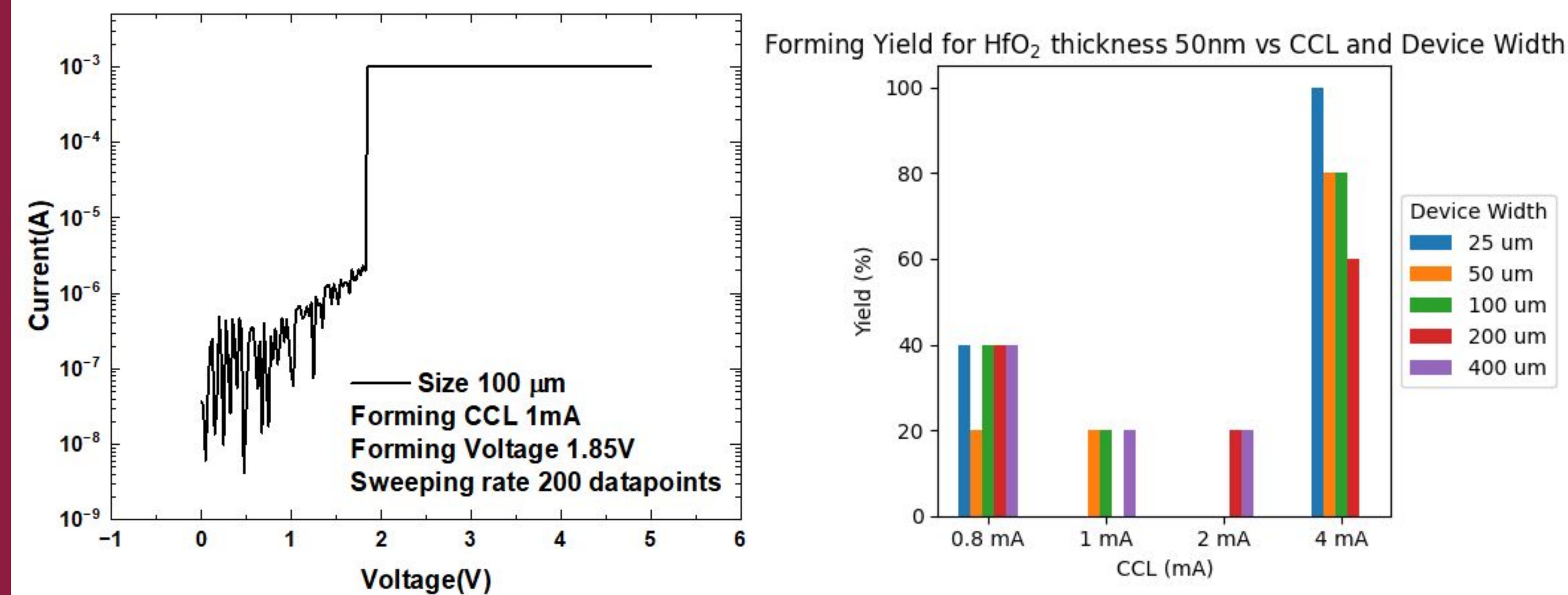
HfO_2 Thickness	50, 100, 200 nm
Device Area (width)	25, 50, 100, 200, 400 um
Total:	75 devices
Best Forming Yield	200nm HfO2
Best Cycling Yield	200nm HfO2



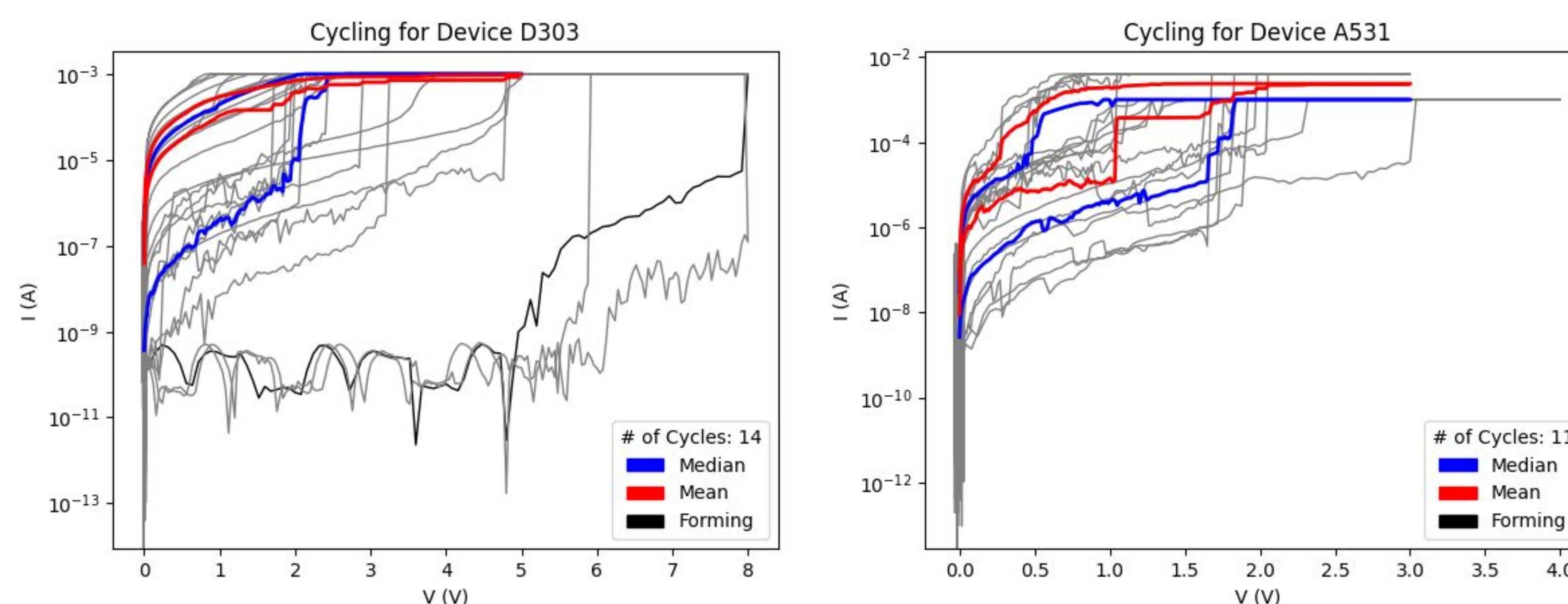
Devices were pre-fabricated and tested in Dr. Chen's GWC 543 lab using an MPS150 probe station and Keysight B1500A semiconductor parameter analyzer (pictured above).

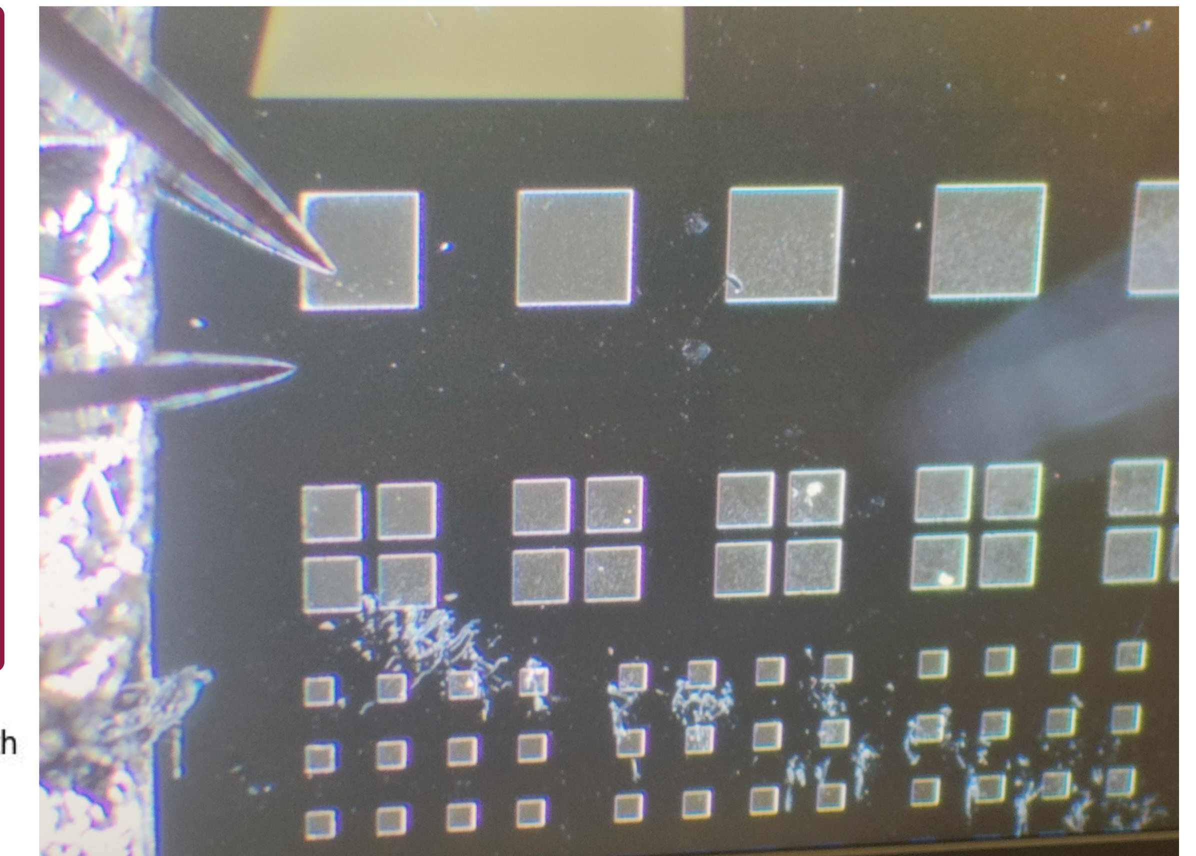
Testing and Results

Forming: A DC voltage sweep is applied with a compliance current limit (CCL). Four CCL levels were tested — 0.8, 1, 2, and 4 mA — to quantify how CCL affects forming yield and filament robustness. Higher CCL produces thicker, more stable filaments but requires more energy to RESET.



SET/RESET cycling: The 200 nm / 25 µm devices showed non-standard switching — requiring very slow (1000–2000 step) voltage sweeps at very low voltages (±200 µV) for reset. Four alternating reset sweeps per cycle were used to reliably destabilize the filament.
Due to extreme sensitivity, resistance reads were taken at 1 mV (vs. typical 100 mV) to prevent unintended switching.





Conclusion

This project successfully demonstrated repeatable resistive switching in novel Pt/SiO_2/HfO_2/SiO_2/Pt trilayer RRAM devices. Key achievements so far:

- All 75 devices characterized in initial HRS; forming yield confirmed across multiple thicknesses and areas.
- Proof of concept: 1.85 V forming voltage at 1 mA CCL for 100 nm / 100 µm device.
- Over 10 consistent SET/RESET cycles achieved in 200 nm / 25 µm devices.
- Self-compliant reset behavior identified — a potentially novel characteristic of the trilayer structure.
- Forming yield largely independent of CCL and device area.
- 200nm HfO_2 thickness had highest forming and switching yield.