

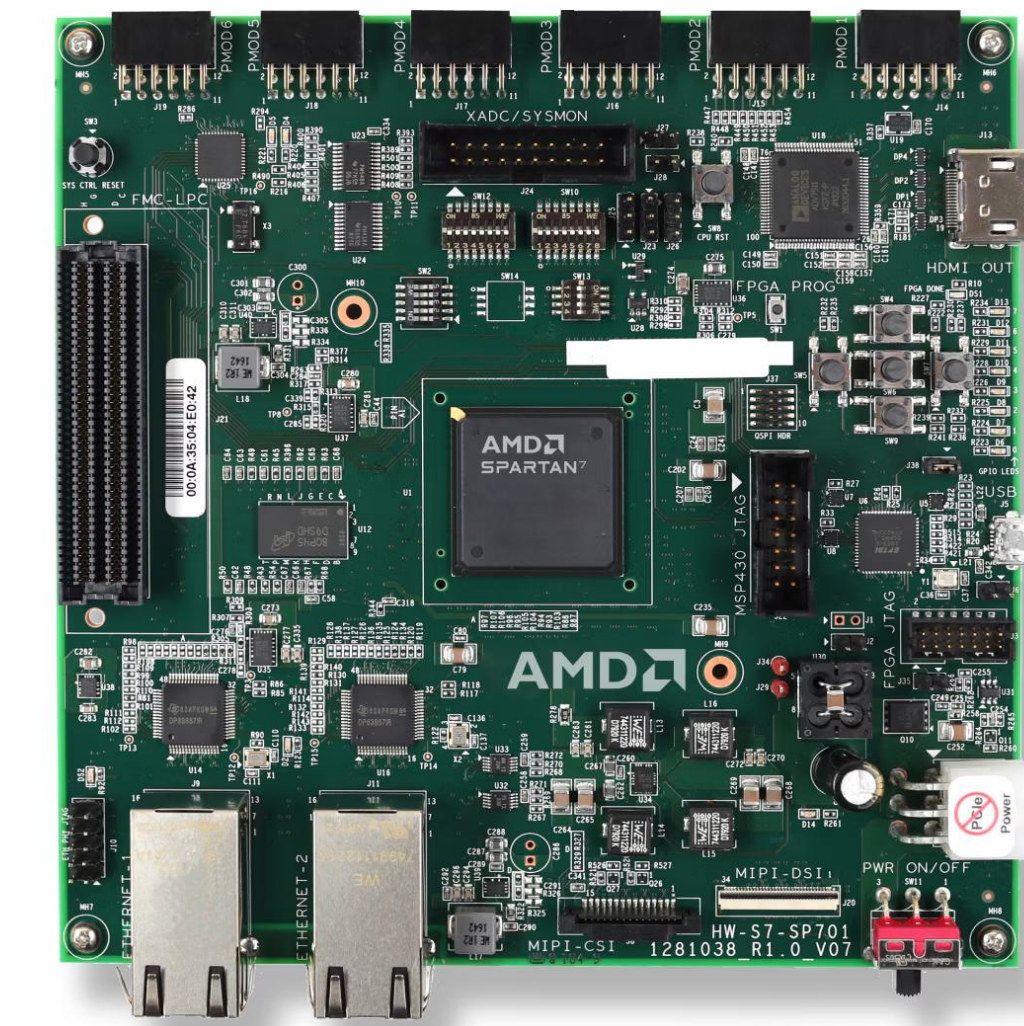
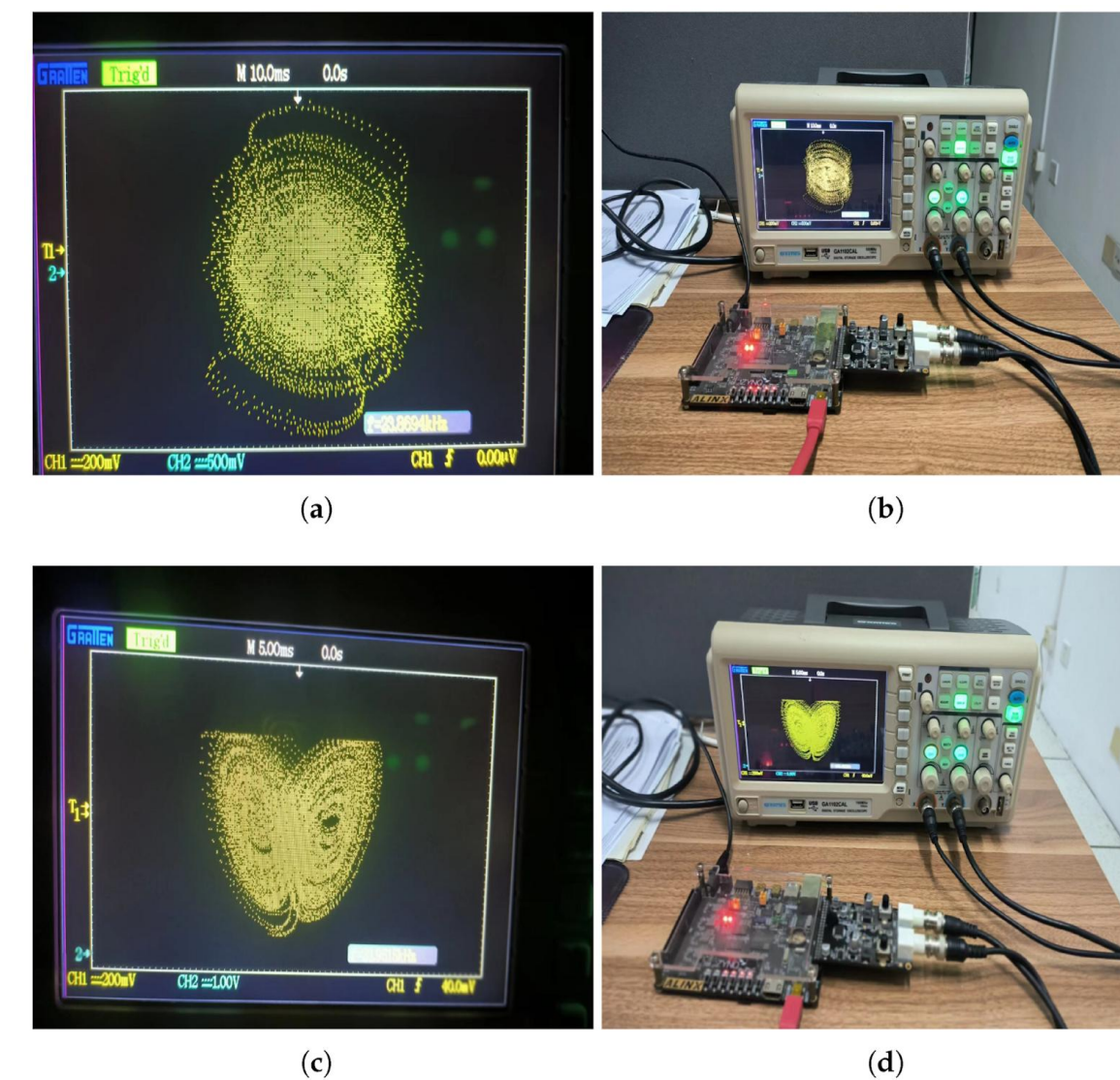
Simulating Differential Equations Using FPGAs

Spring 2026 E.E. Capstone Showcase

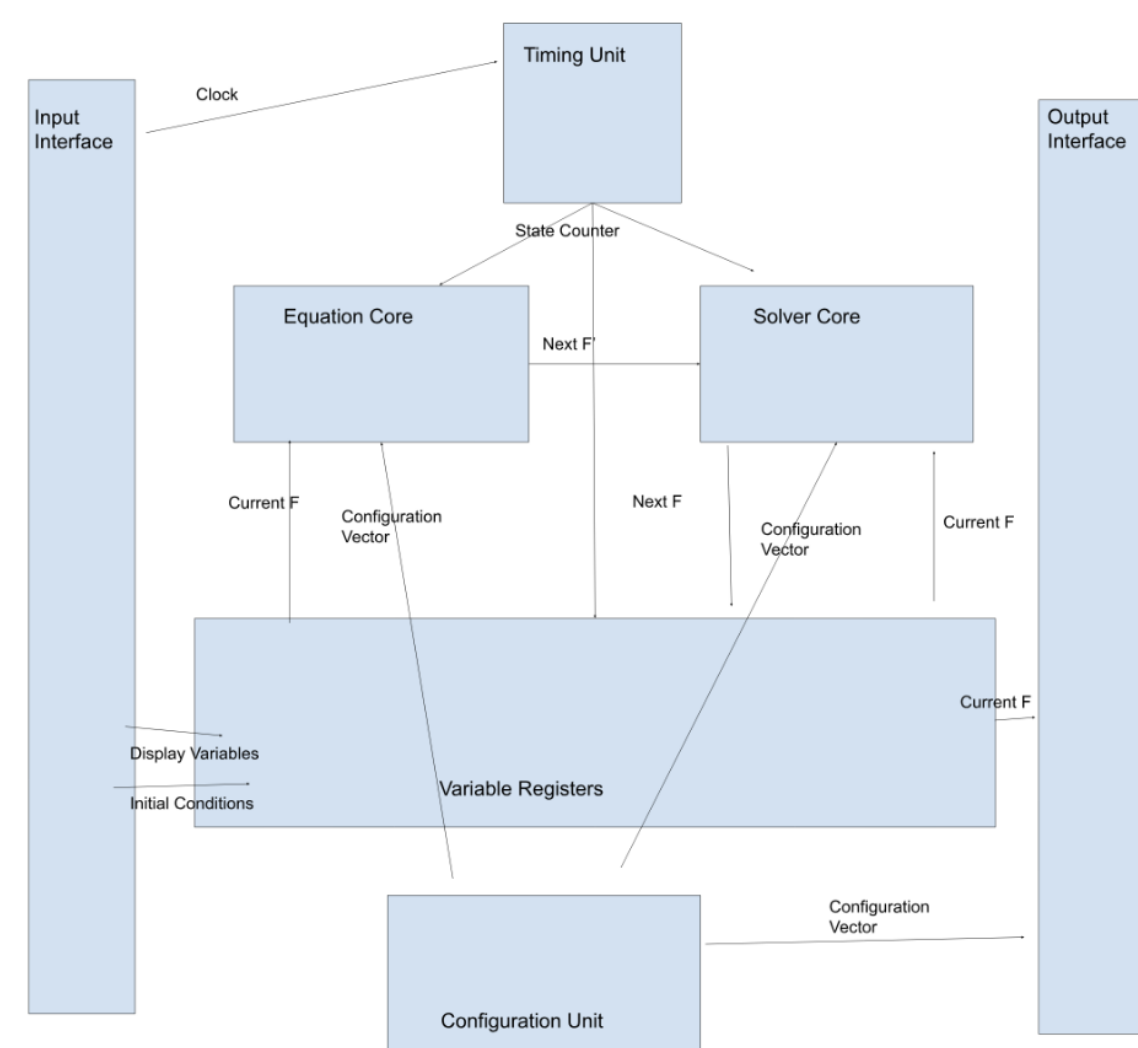
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What We Are Achieving

The primary goal of Team 32 is to create a high-speed, real-time simulation platform that transforms abstract differential equations into tangible, observable signals. By implementing numerical solvers directly on FPGA hardware, the team aims to provide a modular and interactive tool that demonstrates the practical convergence of mathematics and digital design to inspire students entering STEM fields.



Architecture



Main Components

- AMD Spartan-7 XC7S50 FPGA
- Runge-Kutta Solver Cores
- Equation Cores
- Timing and Configuration Units
- VGA and Oscilloscope Interfaces
- USB-to-RS-232 Communication Bridge
- 50 MHz Oscillator
- 12V to 5V/1.0V Power Regulation System
- Digital Output Buffers

System Capabilities

- RTL Synthesis: Translated continuous differential equations into discrete, real-time hardware logic.
- Parallel Processing: Executing solver algorithms at 50 MHz to bypass sequential software delays.
- Full Integration: Bridged custom power, core logic, and display interfaces for live visualization.

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