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Team 17
Automated Test Instrumentation System

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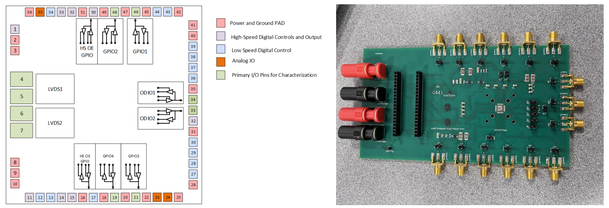
CERTUS semiconductor
CUSTOM IO AND ESD SOLUTIONS

Introduction



Layout of S90 test-chip

Prototype Board for Test Chip

What is test bench automation w/ pyvisa?

- A Python testbench automation package that, in itself, is a wrapper of IVI Visual Instruments Software Architecture Library (VISA).
- pyvisa allows control of equipment that have VISA backends which will allow for automation of test bench equipment.
  - Such equipment include Oscilloscopes, multimeters, power supplies, and more.

Advantages

- Streamlines technical standardization of products with automated testbenches
- Changes in equipment is near plug 'n' play due to pyvisa modules communicate with equipment via Standard Commands for Programmable Instruments (SCPI)

Testbench realization will be completed in partnership with Certus Semiconductor.

- Testbench will be designed to capture characteristics from Certus Semiconductors S90 MPW which is contained within the Certus S90 Test Plan.
- S90 MPW is a Certus's small test chip that will be characterized automatically
  - S90 MPW contains two General Purpose Input/outputs (GPIO), two Low Voltage Differential Signaling IO (LVDS), and two Open-Drain Input-Output (ODIO)

Theory

Test Equipment

- The multimeter, oscilloscope, and waveform generator are communicated with using daisy-chained GPIB connectors
- The Python module PyVisa is used to pass binary ASCII (SCPI) commands to the addressed equipment.
- Proper considerations must be made to ensure ample time to receive commands, and to eliminate cross-talk.
  - Cable length, # of connections, delay between commands, etc.

Transmission Lines

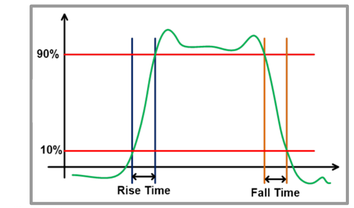
- Because of the high-frequency nature of some tests, all cables and connectors are standardized to 50 ohms.
- This is important to minimize reflections and maximize the authenticity of measurements taken.

Results

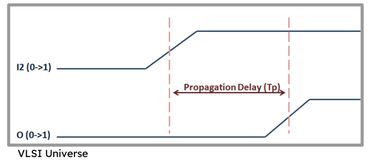
Certus Semiconductor Inc. has been provided with a testbench capable of several important characterizing measurements for GPIO, ODIO, and LVDS interfaces, such as::

- Rise and fall time
- Propagation delay
- Voltage input low and high
- Current output low and high
- Analog MUX resistance

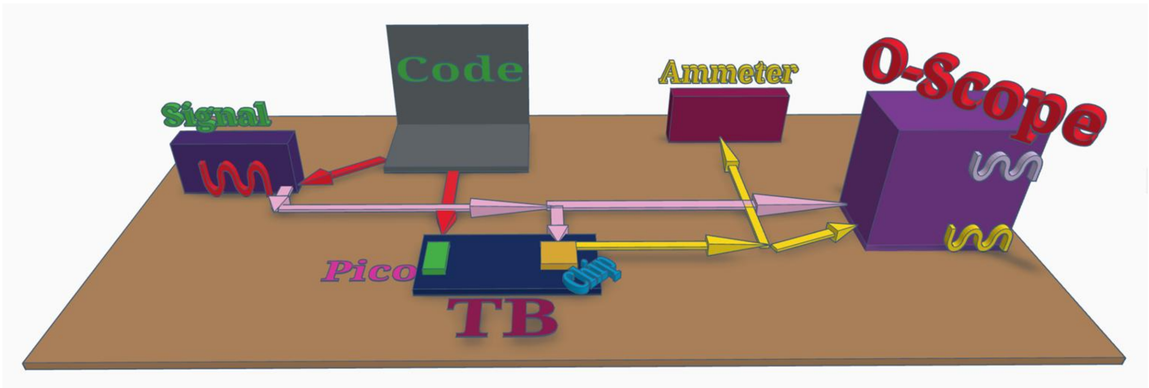
Results are derived from the testbench as illustrated below. A test plan was provided from Certus Semiconductor, and the design of the testbench was created to meet each specification. Our team is confident in the ability of the system to accurately measure and report data as required.



Electrical4U



VLSI Universe



Flowchart illustrating signal and data flow

Conclusion

This project aims to create a testbench to characterize the S90 I/O test library provided by Certus for their use in their own facility. This testbench will be automated to determine characteristics of chips such as propagation delays, rise and fall times, etc. In-house testing is a valuable asset for Certus in terms of production time and cost for future chips. In collaboration with the Team 14, the prototype board and test chips were seamlessly inserted into the testbench design and thoroughly tested to validate the effectiveness of the setup.