Simulation & Modeling of MRAM for On-Chip Learning

Ira A. Fulton Schools of Engineering
Arizona State University

Team 12: Selin Bakkaloglu, Jonathan Rossman, Caidyn Spickler, Elliot Word
Mentor: Prof. Deliang Fan
School of Electrical, Computer, and Energy Engineering




Introduction

- AI models require high memory bandwidth and power, keeping them dependent on cloud computing.
- A conventional CPU cannot support these workloads locally, creating a need for hardware that enables fully on-chip learning.
- MRAM is a promising **non-volatile memory** for this purpose, using a Magnetic Tunnel Junction (MTJ) to store data through resistance changes (Fig. 2).
- An MTJ consists of a pinned layer and a free layer, and their magnetic alignment determines the stored bit (Fig.1) :

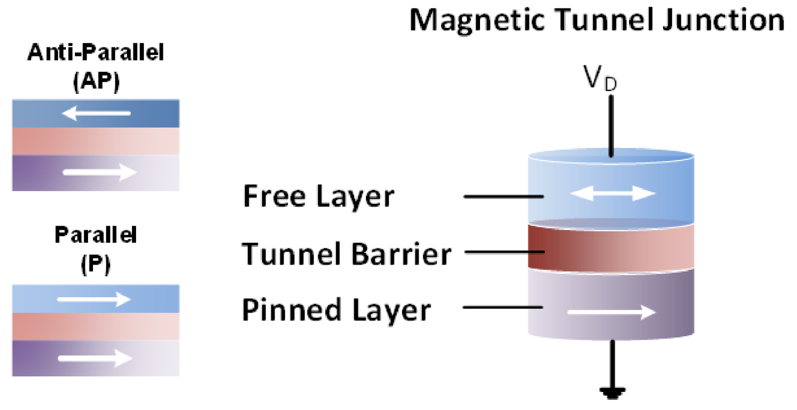


Figure 1. MTJ Parallel and Antiparallel States & MTJ Structure

- The parallel stores a “1”, while the antiparallel state stores a “0”.
- Switching the free layer requires spin-polarized current and enables different device types: **STT-MRAM, SOT-MRAM, and the hybrid SAS-MRAM**.

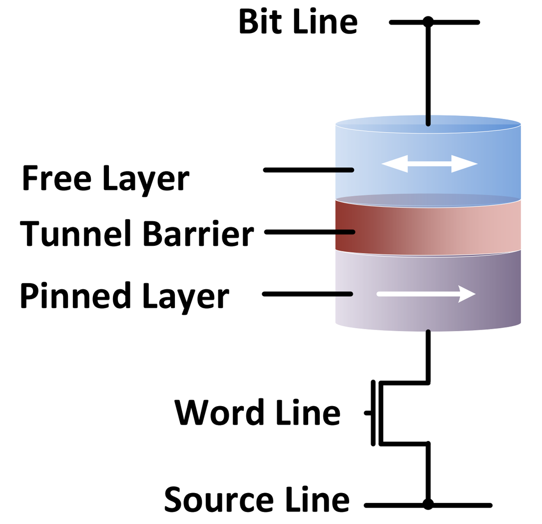


Figure 2. STT-MRAM Cell Structure

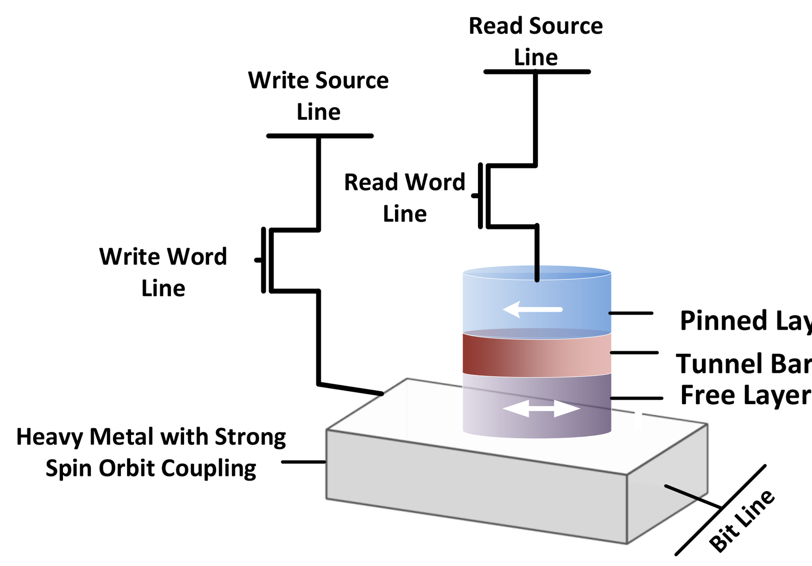


Figure 3. SOT-MRAM Cell Structure

Methods

OOMMF (Object Oriented Micro-magnetic Framework)

- OOMMF, an open source-modeling tool from NIST, was used to simulate the micromagnetic behavior of the MTJ free layer.
- Used to model MTJ switching by numerically solving the Landau-Lifshitz-Gilbert (LLG) equation with spin torque terms.

$$dmdt = -|\gamma| m \times H_{eff} + \alpha\left(m \cdot \frac{\mathrm{d}m}{\mathrm{d}t}\right) + |\gamma|\beta_{\varepsilon}(m \times m_p \times m) - |\gamma|\beta_{\varepsilon}{}' m \cdot m_p$$

Figure 4. LLG equation with spin torque terms used for MTJ Modeling

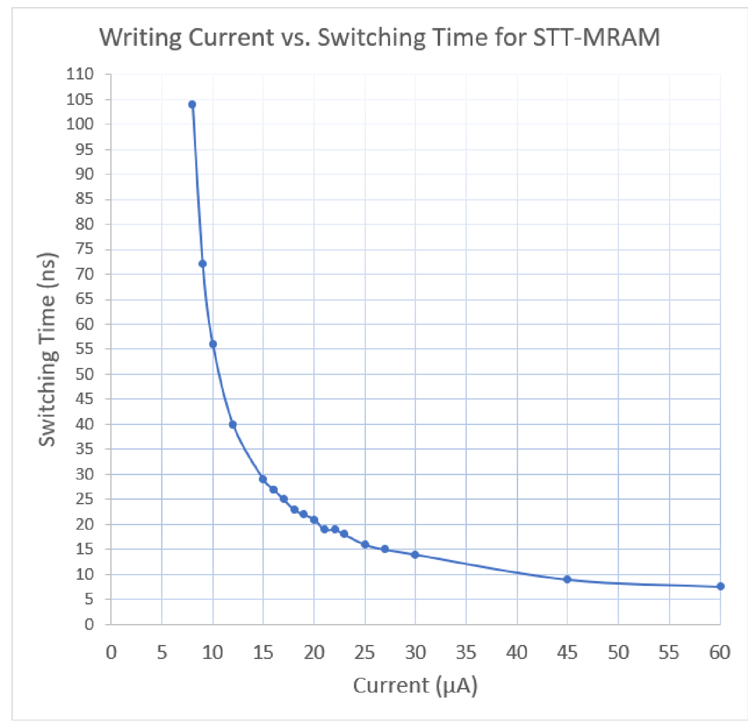
HSPICE

- Used MTJ models to simulate STT, SOT, and SAS write and read operations and verify full magnetization reversal and read stability.

Results

OOMMF

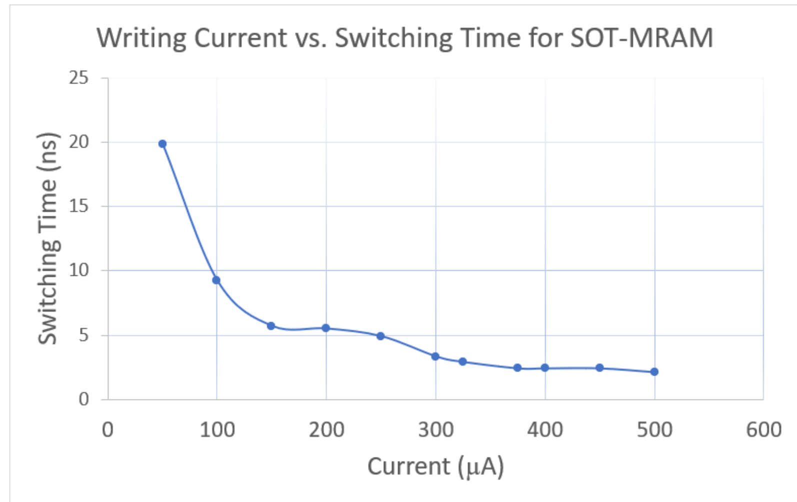
A



A. STT-MRAM Switching Results

- Using OOMMF, the **28 nm STT-MRAM** model demonstrated a critical switching current of **21μA**, with the free layer switching polarity at **19ns.**
- Behavior reflects the expected current-dependent reduction in switching time and confirms efficient operation at relatively low write currents.

B



B. SOT-MRAM Switching Results

- The SOT-MRAM model, which included a **28 nm MTJ** and a 30 × 60 × 7.5 nm heavy-metal layer, required a higher critical current of **150μA** but achieved a free-layer switch in just **5.7 ns**.
- This faster response highlights the performance advantage of SOT-based switching despite its higher current demand.

HSPICE

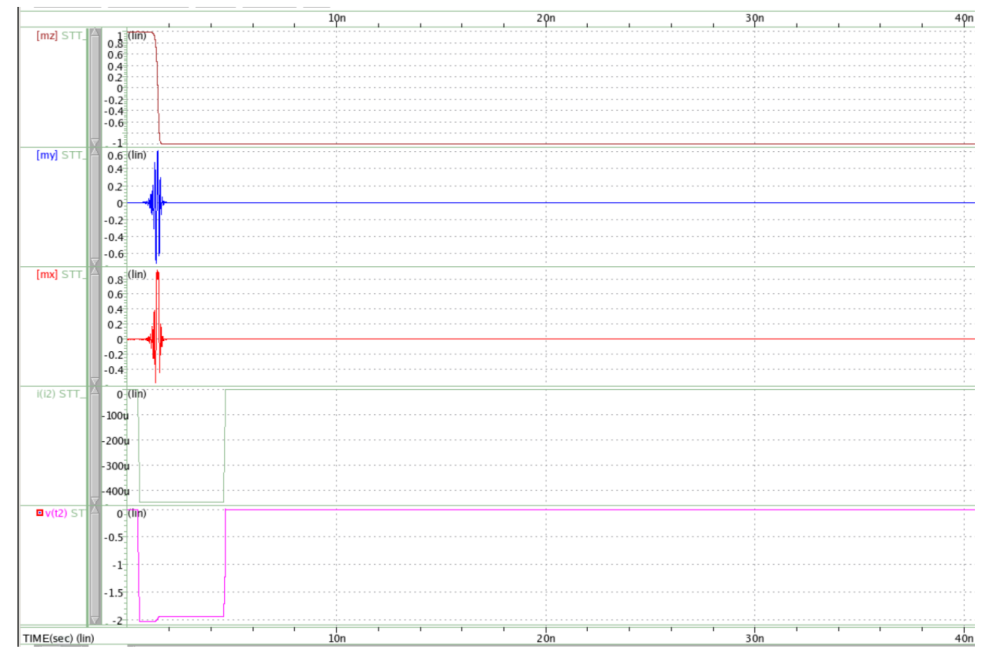
- HSPICE simulations verified that all three MRAM configurations (SOT, STT, and SAS) perform stable and complete write switching, with the free-layer magnetization fully reversing and orthogonal components settling to zero.

C

C. SOT-MRAM HSPICE Results

- With a **450 μA SHE pulse applied over 3.5ns**, the SOT-MRAM device exhibits fast, deterministic switching and smooth settling of all magnetic components.
- No oscillations or metastability appear in the waveform, demonstrating stable spin–orbit torque behavior.

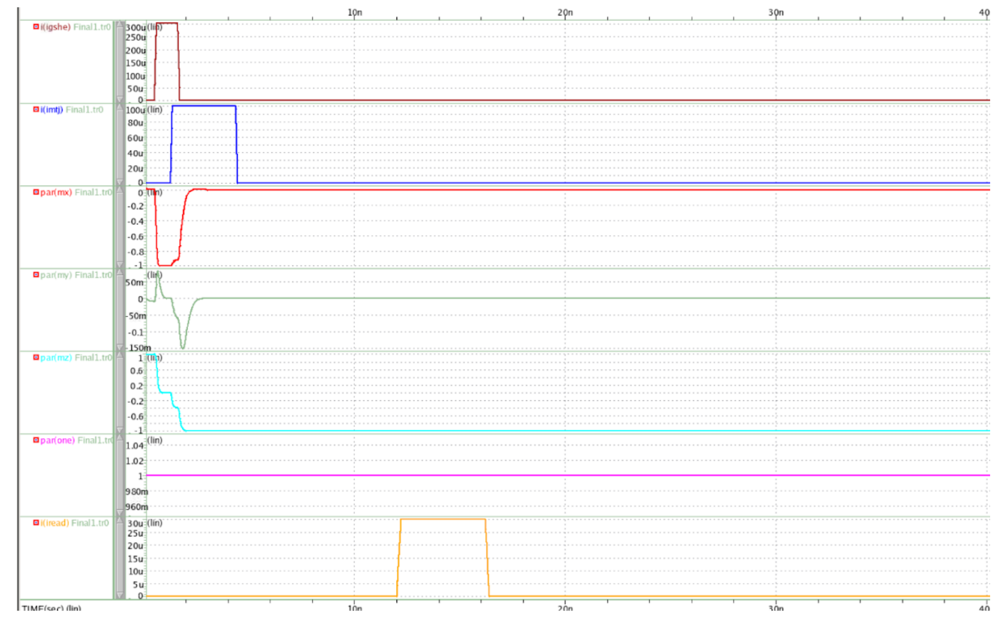
D



D. STT-MRAM HSPICE Results

- The STT-MRAM device successfully switched from the parallel (P) to antiparallel (AP) state when driven with a **–0.45 mA write current** applied over **a 4 ns pulse**.

E



C. SAS-MRAM HSPICE Results

- The SAS-MRAM waveform demonstrates successful switching using a **combined 1 ns SOT pulse (300 μA)** followed by a **3 ns STT pulse (100 μA)**.

Conclusion

- OOMMF provides detailed micromagnetic insight into MTJ switching behavior and field dynamics and HSPICE validates device operation by demonstrating reliable switching and performance.
- Combined, these results show that SAS-MRAM is a viable next step for future on-chip computing architectures.
- Future work would involve integrating these architectures into a DNN memory alongside a volatile memory (SRAM) to have a fully functional AI model for operation in multiple systems.

References

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