Team 17: Sparky’s IC Designers

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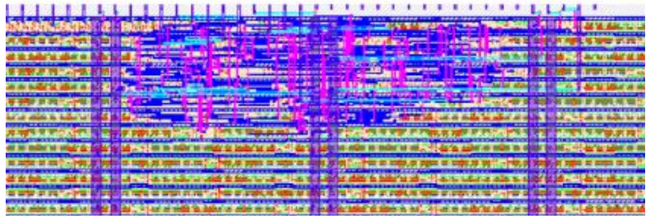
ASIC Fabrication



The figure above shows a gate level diagram of the SAR that would be printed on our ASIC (Application Specific Integrated Circuit). We used Tiny Tapeout, an educational project that allows individuals to easily and affordably design and manufacture custom digital circuits on real chips.

Arduino ASIC Stand-In

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Cycles: 18 Approximated Value: 159  | Actual Value: 159
Cycles: 19 Approximated Value: 175  | Actual Value: 175
Cycles: 19 Approximated Value: 175  | Actual Value: 175
Cycles: 16 Approximated Value: 175  | Actual Value: 175
Cycles: 22 Approximated Value: 175  | Actual Value: 175
Cycles: 18 Approximated Value: 187  | Actual Value: 187
Cycles: 20 Approximated Value: 187  | Actual Value: 187
Cycles: 19 Approximated Value: 187  | Actual Value: 187
Cycles: 18 Approximated Value: 187  | Actual Value: 187
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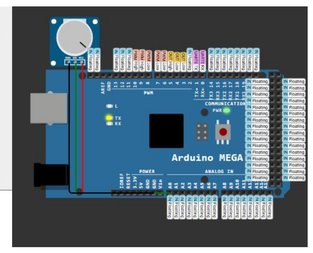


We used an Arduino to model the Successive Approximation Register (SAR) that would’ve been our ASIC manufactured by Tiny Tapeout. Code outputs are shown above.

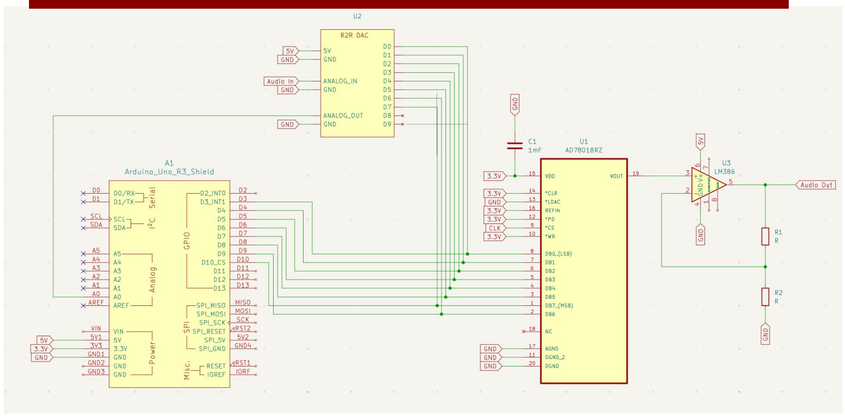
Software Model

A software model was developed to further illustrate the capabilities of non-linear sampling. The Python code simulates different quantization behaviors and visualizes signal compression effects.

Abstract

This project explores the use of open-source tools to design, simulate, and prototype custom integrated circuits at low cost. An 8-bit SAR ADC and support circuitry were developed using Icarus Verilog, KiCad, Qspice, Arduino, and Python. We aim to make chip development more accessible to students, researchers, and small companies.

Hardware Model



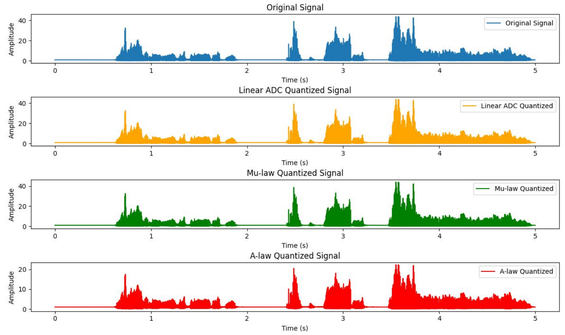
Block Diagram

This physical build uses an Arduino Mega, an R-2R ladder, a comparator, and a DAC to recreate the SAR ADC system and output audio. This setup models real-time nonlinear sampling and demonstrates the SAR’s functionality.

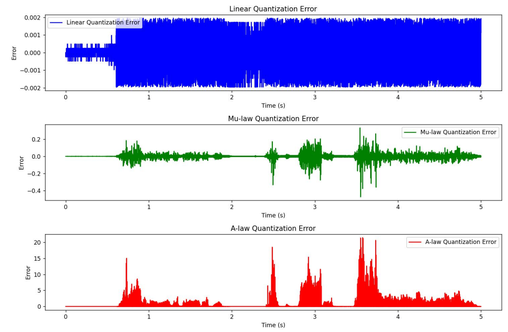
Acknowledgement

Special thanks to Mr. Jim Doyle and Dr. Hongbin Yu for their support and guidance. We also acknowledge the previous capstone team, whose documentation and work inspired our pursuit of open-source chip design.

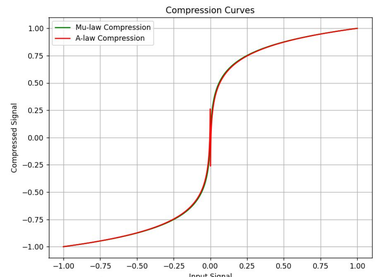
Software Model - Output



Plot of relative signal amplitude over time for different kinds of companding



Plot of quantized error for different types of companding



Plot containing the compression curves of both nonlinear companding algorithms

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